

REMARKS

Claims 1-11, 13-18, 20-21, 23-49, 51-52, and 57-59 were previously pending in this patent application. Claims 1-11, 13-18, 20-21, 23-49, 51-52, and 57-59 stand rejected. Herein, no Claim has been amended. Accordingly, after this Amendment and Response After Final Action, Claims 1-11, 13-18, 20-21, 23-49, 51-52, and 57-59 remain pending in this patent application. Further examination and reconsideration in view of the claims, remarks, and arguments set forth below is respectfully requested.

Specification

The Specification has been amended to correct several figure numbers.

35 U.S.C. Section 103(a) Rejections

Claims 1-11, 13-18, 20-21, 23-49, 51-52, and 57 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Insenser Farre et al., U.S. Patent No. 6,460,172 (hereafter Insenser) in view of Furtek et al., U.S. Patent No. 5,894,565 (hereafter Furtek) and in view of van der Wal et al., U.S. Patent No. 6,188,381 (hereafter van der Wal) . These rejections are respectfully traversed.

Independent Claim 1 recites (as amended):

A microcontroller circuit comprising:
a bus;
a microprocessor coupled to said bus;

a memory coupled to said bus, wherein said memory comprises a non-volatile memory; and

a plurality of functionalities coupled to said bus, wherein said non-volatile memory functions to program said functionalities and wherein said plurality of functionalities comprise:

an interconnect wherein said interconnect is dynamically configurable and programmable;

an analog functional block coupled to said interconnect wherein said analog function block is dynamically configurable and programmable to perform one or more of a plurality of various analog functions; and

a dynamically configurable and programmable digital functional block coupled to said interconnect, wherein said dynamically configurable and programmable digital functional block ***is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation.*** (emphasis added)

It is respectfully asserted that the combination of Insenser, Furtek, and van der Wal does not teach, suggest, or motivate the present invention as recited in Independent Claim 1. In particular, Independent Claim 1 recites the limitation, "said dynamically configurable and programmable ***digital functional block is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation,***" (emphasis added). This Final Office Action maintains and incorporates by reference the rejections stated in the Office Action mailed 4/26/06. At page 5 of the Office Action mailed 4/26/06, it is stated that neither Insenser nor Furtek specifically shows the single register write operation as claimed in Independent Claim 1. Further, it is argued at page 5 of the Office Action mailed 4/26/06 and at page 3 of the Final Office Action that van der Wal teaches a reconfigurable system (or device) including (or having) a single control register write for reconfiguring all functional blocks or devices, citing Col. 10, lines 30-38 of van der Wal.

The passage (Col. 10, lines 30-38) of van der Wal recites:

data for each channel. These 10 bits represent the 8 bits of data and 2 bits of HA and VA timing in the format described above. In a preferred embodiment, the crosspoint switch 202 is implemented using 10 I-CUBE IQ96 crosspoint switch devices. Each of these devices provides a reconfigurable crosspoint ***switch for a single bit of the 10 bits of video data***. These devices are configured ***so*** one control register write ***is capable of switching all*** 10 bits of data in all 10 IQ96 devices ***simultaneously***. (emphasis added)

This passage has been misinterpreted as teaching the configuration or reconfiguration of a device with a single register write, as in Independent Claim 1. Rather, the passage is directed to one control register write that is capable of switching all bits of video data in all devices simultaneously.

According to the passage, 10 (ten) I-CUBE IQ96 crosspoint switch devices implement the crosspoint switch 202. Moreover, each I-CUBE IQ96 crosspoint switch device provides a reconfigurable crosspoint switch for a single bit of the 10 bits of video data. Further, the 10 (ten) I-CUBE IQ96 crosspoint switch devices are configured as a whole in a manner described by the phrase which begins after the word "so" in the last sentence of the passage. That is, the phrase, "one control register write is capable of switching all 10 bits of [video] data in all 10 IQ96 devices simultaneously" (emphasis added), refers to the operation of the 10 (ten) I-CUBE IQ96 crosspoint switch devices as a whole. Thus, there is no support for the assertion made in the Office Action mailed 4/26/06 and in the Final Office Action that the passage teaches, "single control

register write for reconfiguring all functional blocks or devices". The one control register write in the passage is described as being capable of switching all 10 bits of video data in all 10 IQ96 devices simultaneously instead of reconfiguring functional blocks or devices. While the passage notes that bits of video data are switched simultaneously with the one control register write, the passage fails to describe any relationship between the one control register write and configuration (or reconfiguration) of the individual I-CUBE IQ96 crosspoint switch device. Use of the term "switching" corresponds to each I-CUBE IQ96 crosspoint switch device having an "on state" and an "off state". Therefore, each I-CUBE IQ96 crosspoint switch device must be configured/reconfigured with respect to its input and output ports via its corresponding control register in some manner that is neither described nor expressly/implicitly referred as being a single control register write. Thus, van der Wal does not teach, suggest, or motivate that a digital functional block is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation, as in the invention of Independent Claim 1.

At page 3 of the Final Office Action, "function" is read as any path connection because it is asserted that "function" is neither clearly defined in the specification nor in the claim. Applicant respectfully disagrees with this assertion and reading of the word "function". It is respectfully submitted that the meaning of "analog function" is provided through examples on pages 27-28 of the specification and that the meaning of "digital function" is provided through examples on pages 44-45 of the specification.

As described above, the combination of Insenser, Furtek, and van der Wal does not teach, suggest, or motivate all the limitations of Independent Claim 1. Therefore, it is respectfully submitted that Independent Claim 1 is patentable over the combination of Insenser, Furtek, and van der Wal and is in condition for allowance.

Dependent Claims 2-10 are dependent on allowable Independent Claim 1, which is allowable over the combination of Insenser, Furtek, and van der Wal. Hence, it is respectfully submitted that Dependent Claims 2-10 are patentable over the combination of Insenser, Furtek, and van der Wal for the reasons discussed above.

With respect to Independent Claims 11, 17, 35, 37, 42, 51, and 52, it is respectfully submitted that Independent Claims 11, 17, 35, 37, 42, 51, and 52 recite similar limitations as in Independent Claim 1. In particular, Independent Claims 11, 17, 35, 37, 42, 51, and 52, are directed to digital logic whose digital function is "configured ***with a single register write operation***," (emphasis added). The combination of Insenser, Furtek, and van der Wal does not teach, suggest, or motivate all the limitations of Independent Claims 11, 17, 35, 37, 42, 51, and 52. Therefore, it is respectfully submitted that Independent Claims 11, 17, 35, 37, 42, 51, and 52 are patentable over the combination of Insenser,

Furtek, and van der Wal and are in condition for allowance for reasons discussed in connection with Independent Claim 1.

Dependent Claims 13-16, 18, 20-21, 23-34, 36, 38-41, 43-49, and 57 are dependent on allowable Independent Claim 11, 17, 35, 37, 42, 51, and 52, which are allowable over the combination of Insenser, Furtek, and van der Wal.

Hence, it is respectfully submitted that Dependent Claims 13-16, 18, 20-21, 23-34, 36, 38-41, 43-49, and 57 are patentable over the combination of Insenser, Furtek, and van der Wal for the reasons discussed above.

Claims 58-59 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Insenser Farre et al., U.S. Patent No. 6,460,172 (hereafter Insenser) in view of Gamal et al., U.S. Patent No. 5,754,826 (hereafter Gamal) and in view of van der Wal et al., U.S. Patent No. 6,188,381 (hereafter van der Wal). These rejections are respectfully traversed.

Independent Claim 58 recites (as amended):

In a system disposed in an integrated circuit, said system comprising:

- a microcontroller comprising a non-volatile program memory;
- a subsystem coupled to said non-volatile program memory, comprising a plurality of analog functionalities and of digital functionalities that are both configurable according to a user input wherein said analog functionalities are programmable to perform one or more of a plurality of various analog functions and wherein said analog functionalities and said digital functionalities are programmed with code stored in said non-volatile program

memory, wherein each digital functionality ***is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation***;

an interconnecting mechanism configurable for selectively interconnecting said plurality of analog functionalities and said plurality of digital functionalities according to said user input; and

a coupling mechanism coupled to said subsystem that is configurable to implement a connectability state for said system by which said system is connectable to an external entity according to said user input, a method of configuring said system comprising:

a) selecting a function from the list consisting of analog functions, digital functions, and; mixed analog and digital functions

b) selecting an interconnection state to effectuate an interconnection between said analog functionalities and said digital functionalities corresponding to said function;

c) selecting said connectability state to effectuate an connection between said system and an external entity corresponding to said function; and

d) implementing said function, said interconnection state, and said connectability state according to said a), said b) and said c). (emphasis added)

It is respectfully asserted that the combination of Insenser, Gamal, and van der Wal does not teach, suggest, or motivate the present invention as recited in Independent Claim 58. In particular, the Independent Claim 58 recites the limitation, "each digital functionality ***is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation***," (emphasis added). At page 23 of the Office Action mailed 4/26/06, it is stated that neither Insenser nor Gammal specifically shows the single register write operation as claimed in Independent Claim 58. Further, it is argued at pages 23-24 that van der Wal teaches a reconfigurable system including a single control register write for reconfiguring all functional blocks or devices, citing Col. 10, lines 30-38 of van der Wal. For the reasons explained above with respect to Independent Claim 1, van der Wal does not

teach, suggest, or motivate that each digital functionality is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation, as in the invention of Independent Claim 58.

As described above, the combination of Insenser, Gamal, and van der Wal does not teach, suggest, or motivate all the limitations of Independent Claim 58. Therefore, it is respectfully submitted that Independent Claim 58 is patentable over the combination of Insenser, Gamal, and van der Wal and is in condition for allowance.

Dependent Claim 59 is dependent on allowable Independent Claim 58, which is allowable over the combination of Insenser, Gamal, and van der Wal. Hence, it is respectfully submitted that Dependent Claim 59 is patentable over the combination of Insenser, Gamal, and van der Wal for the reasons discussed above.

CONCLUSION

It is respectfully submitted that the above claims, arguments and remarks overcome all rejections and objections. All remaining claims (Claims 1-11, 13-18, 20-21, 23-49, 51-52, and 57-59) are neither anticipated nor obvious in view of the cited references. For at least the above-presented reasons, it is respectfully submitted that all remaining claims (Claims 1-11, 13-18, 20-21, 23-49, 51-52, and 57-59) are in condition for allowance.

The Examiner is urged to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 23-0085.

Respectfully submitted,

WAGNER, MURABITO & HAO, LLP

Dated: 10/10/2006 Jose S. Garcia

Jose S. Garcia
Registration No. 43,628

Two North Market Street, Third Floor
San Jose, CA 95113
(408) 938-9060